REMARKS

Claims 1-21 were examined. Claims 1, 4, 10 and 14 are amended. Claims 7-9 and 17-21 are canceled. Claims 22 and 23 are added. Claims 1-6, 10-16 and 22-23 remain in the Application.

In an Office Action dated July 28, 2005, the Patent Office rejected claims 1-21 under 35 U.S.C. §103(a). Reconsideration of the pending claims is respectfully requested in view of the above amendments and the following remarks.

A. 35 U.S.C § 103(a): Rejection of Claims 1-4, 7-14, 17-18 & 21

The Patent Office rejects claims 1-4, 7-14, 17-18 and 21 under 35 U.S.C. §103(a) as obvious over Erikson.

Erikson discloses an ultrasound transducer array using multilayer structures composed of active and passive devices. The technique can be exploited in an acoustical ray assembly to isolate transmit and receiving circuitry for improved performance, as well as to provide higher density packaging, mixing of alternate IC fabrication techniques and other related advantages. Column 10 lines 51-55. Figure 5 shows an embodiment wherein high and low voltage circuitry is segregated in integrated circuit layer 20 and integrated circuit layer 30, respectively. Figure 6-9 shows similar structures.

Independent claim 1 is not obvious over Erikson, because Erikson does not describe or provide motivation for an apparatus comprising a semiconductor die, a first package substrate electrically coupled to a plurality of interconnects on a front side of the die and a second package substrate electrically coupled to a plurality of interconnects on a back side of the die, wherein a portion of at least one of a power requirement and an external signal requirement (e.g., I/O signal) is supplied through the first package substrate and a remainder portion of at least one of the power requirement and the external signal requirement is supplied through the second package

substrate. Erikson is directed at isolating circuits on various substrates, such as isolating high voltage and low voltage circuits. In fact, the reference by the Patent Office to integrated circuit wiring elements such as power supplies and grounds at column 11, lines 1-4 is not described in Erikson.

Claims 2-4 depend from claim 1 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 1, claims 2-4 are not obvious over Erikson.

Independent claim 10 is not obvious over Erikson, because Erikson does not describe forming a plurality of conductive through vias in a back side of a die including active circuitry on a front side and attaching interconnects to respective ones of the plurality of through vias; coupling a plurality of second interconnects to a front side of the die and electrically coupling the first interconnects to a first substrate and the second interconnects to a second substrate, wherein a portion of at least one of a power requirement of the die and an external signal requirement of the die is supplied through the first substrate and a remainder portion of at least one of the power requirement and the external signal requirement is supplied through the second substrate. As noted above with respect to claim 1, Erikson does not describe apportioning power and/or external signals between substrates.

Claim 14 depends from claim 10 and therefore contains all the limitations of that claim. For at least the reason stated with respect to claim 10, claim 14 is not obvious over Erikson.

Applicant respectfully request that the Patent Office withdraw the rejection to claims 1-4, 10 and 14 under 35 U.S.C §103(a).

B. 35 U.S.C § 103(a): Rejection of Claims 5, 15 & 19

The Patent Office rejects claims 5, 15 & 19 under 35 U.S.C § 103(a) as obvious over Erikson and further in view of U.S. Patent Number 5,811,877 Miyano, et al. (Miyano). Miyano is cited for disclosing the thinning of or etching of chips in a stacked package in order to prevent cracking.

Claims 5 and 15 depend from claims 1 and 10, respectively, and therefore contain all the limitations of those claims. For at least the reasons stated with respect to claims 1 and 10, claims 5 and 15 are not obvious over the cited references. The addition of teachings of thinning does not complete the requirements of all the elements in claims 5 and 15. Applicant respectfully requests the Patent Office withdraw the rejection to claims 5 and 15 under 35 U.S.C §103(a).

C. 35 U.S.C.§ 103(a): Rejection of Claims 6,16 & 20

The Patent Office rejects claims 6, 16 & 20 under 35 U.S.C § 103(a) as obvious over Erikson in view of U.S. Patent Number 5,855,821 of Chau, et al. (Chau). Chau is cited for disclosing controlled collapse chip connection and a dam.

Claims 6 ad 16 depend from claims 1 and 10, respectively, and therefore contain all the limitations of those claims. For at least the reasons stated with respect to claims 1 and 10, claims 6 and 16 are not obvious over the cited references. The addition of teachings of chip connections and a dam does not overcome the deficiencies in the primary reference Erikson.

The applicant respectfully requests the patent office withdraw the rejection to claims 5 ad 15 under 35 U.S.C §103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 10/25/05

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